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Q64273

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7590 06/15/2007  
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EXAMINER

CHANG, VICTOR S

ART UNIT

PAPER NUMBER

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.



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**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

Application Number: 09/830,605  
Filing Date: April 30, 2001  
Appellant(s): ICHIKAWA ET AL.

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Joseph J. Ruch, Jr.  
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed April 16, 2007 appealing from the Office action mailed August 15, 2006.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

US 6,065,701

Tanimura et al.

5-2000

Applicants' admission, specification, pages 1-2, bridging paragraph.

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

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Claims 1, 2 and 4-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanimura et al. [US 6065701] in view of Applicants' admission.

Tanimura's invention relates to a label comprising an integrated circuit (IC). The IC comprises a memory unit and a signal processing unit [abstract]. Fig. 2 shows that the adhesive label has an antenna wiring (antenna coil) 30 and an IC 20 formed on a polyimide substrate 16, a "both faces adhesive material" (double sided) adhesive layer 17, and an exfoliative paper (release layer) 18. The adhesive layer 17 adheres the label to a video cassette tape [column 4, lines 7-8]. The label has a coated paper layer 12 as an outer surface layer for carrying information such as the title, recording date, and recording place [column 3, lines 52-56]. A non-contact (contactless) system is used for transferring data to the memory unit [column 2, lines 15-17].

For claims 1, 2 and 4, Tanimura's IC reads on the instantly claimed data carrier element. Tanimura lacks a teaching that the data carrier element is laminated between the substrate 16 and adhesive layer 17. However, applicants have admitted in the "Background Art" section that while typically an entire contactless data carrier element is formed on one side of the circuit substrate [Fig. 3], alternatively the contactless data carrier element may be prepared by separately forming a part of an electric circuit on each side of the circuit substrate, and connecting one to the other via a through-hole, to thus integrate the separately formed parts (electronic components) [specification, pages 1-2, bridging paragraph]. The examiner interprets applicants' admission as a whole rendering obvious that the electronic components of the data carrier element may be formed on either side of the circuit substrate entirely or partially, and the alternative arrangements functions equivalently, because a specific side of substrate is not required for placing the electronic components. It would have been obvious to one of ordinary

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skill in the art to use an alternative functionally equivalent arrangement of placing the entire data carrier element on the side of the substrate which is in direct contact with the adhesive layer 17, and reads on the instant invention as claimed. It should be noted that the selection of a known equivalent material based on its suitability for its intended use supported a *prima facie* obviousness determination. See MPEP § 2144.07.

For claims 5 and 7, Tanimura's coated paper layer 12 reads on the surface layer as claimed.

For claim 6, applicants' admission renders connecting electronic components of the data carrier element via a through-hole obvious, as set forth above. Regarding the term "surface layer", in the absence of any composition and/or structural limitations of what constitutes a "surface layer", the multilayer structure (layers 12, 13, 14 and 15) of Tanimura reads on the "surface layer" of instant invention as claimed.

For claims 8-14, since they claim the same scope as claims 1, 2 and 4-7, they are also rejected for the reasons as set forth above.

#### **(10) Response to Argument**

Appellants argue at page 13 that the examiner appears to have ignored the plain meaning of the passage (contactless data carrier element may be prepared by separately forming a part of an electric circuit on each side of the circuit substrate, and connecting one to the other via a through-hole) on page 2, lines 2-7 of the present specification, and contend that the passage describes an embodiment having the electric circuit, or data carrier element, formed on both sides of the circuit substrate, which cannot be interpreted as having the data carrier element formed on either side of a substrate and functions equivalently. However, appellants' argument

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ignores that the complete basis of the examiner's reasoning includes appellants' admission that typically an entire contactless data carrier element is formed on one side of the circuit substrate [Fig. 3], and the abovementioned passage admits that electronic components may be placed at either side of the circuit substrate and functions equivalently. The examiner interprets applicants' admission as a whole rendering obvious that the electronic components of the data carrier element may be formed on either side of the circuit substrate entirely or partially, and these alternative arrangements functions equivalently, because a specific side of the substrate is not required for placing the electronic components.

Appellants argue at page 14 that the examiner has improperly interpreted the term "electronic part" is the same as the "electric circuit" at page 4 of Office action mailed 8/15/2006. However, the examiner merely states that "it is inconceivable that an "electric circuit" is not formed of "electronic components", and an "electronic components" would not have contained certain "electric circuit" inside". Nowhere has the examiner made any statement that these terms are the same.

Appellants argue at page 14 that the examiner cannot rely upon a sentence within the specification as the basis for an alleged "admission" but then ignore the subject matter that the sentence actually describes. However, both the relied upon passage and the description of Fig. 3 (prior art) are from the same paragraph and they are entirely contained in the "Background Art" section. Appellants appear to argue that the teachings of embodiments in separate sentences cannot be combined. The examiner asserts that since these embodiments are described in one paragraph as alternative functionally equivalent embodiments, the teachings are combinable and render obvious that the electronic components of the data carrier element may be formed on

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either side of substrate entirely or partially, and these alternative arrangements functions equivalently.

Appellants argue at page 15 that the examiner has not responded to appellants' argument that there is no indication in the abovementioned passage that the adhesive layer 5 can be rearranged in such a manner that would render appellants' invention obvious. However, since the admitted prior art renders obvious that the entire data carrier element may be formed on either side of the circuit substrate, and either Tanimura or Fig. 3 of admitted prior art shows that an adhesive layer is laminated to the circuit substrate, it is unseen how the adhesive layer would not be in direct contact with the entire data carrier element when an obviously functionally equivalent alternative structure (i.e., the entire data carrier element is placed on the side of circuit substrate facing the adhesive layer) is employed.

Appellants argue at pages 19-23 that Yamakage's Declaration shows unexpected remarkable effects obtainable by the present invention over the closest prior art of Tanimura. Specifically, appellants argues that Table 1 of the Declaration shows that the printability of the present invention in Experiment A with a thin adhesive layer is sufficient from a practical standpoint, whereas the Comparative Experiments A-C requires thick adhesive layer. However, the thickness of the adhesive layer is not present in any claims. Further, since the Declaration shows that Comparative Experiment C has better printability than Experiment A, the present invention does not necessarily have a superior printability.

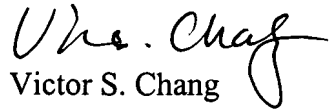
#### **(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

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For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

  
Victor S. Chang

Conferees:

/Jennifer Michener/

Quality Assurance Specialist, TC 1700

  
Terrel Morris